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TITLE: DATA PROCESSOR

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ABSTRACT:

PROBLEM TO BE SOLVED: To provide a data processor in which an interlock period can be shortened and performance can be improved by changing the number of pipeline stages with the change of an operation clock frequency and switching a forwarding path.

SOLUTION: An instruction fetch circuit 31 and an instruction decoding circuit 32 process data at one cycle time. In a data cache 4, access time

changes by the change of the operation clock frequency . In that case, a selector 340 selects load data of one cycle time in the data cache 4 and executes a next processing when a high speed pitch flag 35 is cleared. When it is set, the selector 340 selects load data for the two cycle time of the data cache 4 and executes the next processing. The optimum bypass of data can be selected with the speed change of a clock.